The FPTT Board (DRAFT)

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(Revised)

Introduction

This document provides a description of the algorithm, programming and operation of the forward pre-shower trigger term (FPTT) board in the Dzero L1/L2 trigger. The details of construction and operation of the FPS are described elsewhere (Abid). The detector has two components (North and South) mounted in front of the end calorimeters. Each detector is comprised of 16 sectors which subtend 22.5 degrees in polar angle and covering an azimuth from η=1.6-2.5. Each sector has four active layers (*u,v,u',v'*) of scintillating fibers. A two-radiation length converter separates the "*Mip* layers" (*u,v*) from the "*Sho*wer layers" (*u',v'*). The four layers have 103,103,144,144 fibers respectively. The *Mip* layer signals are split and amplified with two gain factors, so the total number of digitized channels per sector is 782, which are handled by a single analog front-end (AFE) board. The sequential architecture of the L1/L2 FPS trigger is shown in Figure. 1.

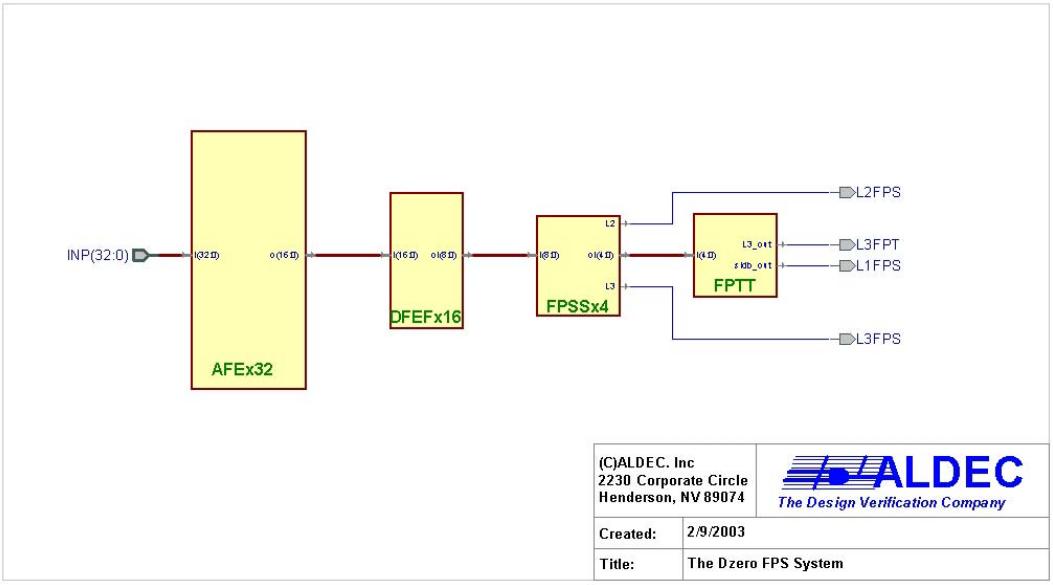

Figure 1 - Block diagram of the FPS trigger components:

The signals from two AFE boards are routed to a single digital front-end board (DFEF). The DFEF boards have two functions: i) Contiguous "hit" fibers in all layers are logically associated as clusters. ii) For each cluster in a *u'* or *v' Sho* layer, a road in the corresponding *u* or *v Mip* layer is searched for a cluster that could have been caused by the same particle. The road is defined as I*Mip* = I*Sho* –4+-3, where I*Mip* and I*Sho* are the *Mip* and *Sho* layer indicies respectively.

The output of the DFEF is an exclusive list of all clusters in the *Sho* layer both with and without a correlated *Mip* layer cluster. Next in the chain is the FPSS board that receives the outputs from four DFEF boards corresponding to half of a N/S detector. The FPSS combines the respective cluster lists and transmits L1+L2 events to the FPTT. It also sends a copy of all L1 events to crate 0x13 (L3) and sends L2 events to the L2FPSpp (pre-processor). Finally, the single FPTT board collects frames from four FPSS cards. It sends trigger terms to the L1 Trigger Manager, and forwards copies of the L2 events to crate 0x13.

The FPTT board receives LVDS signals from the four FPSS boards, and transmits the processed L2 cluster information to crate 0x13 via optical fibers. The L1 records are transmitted to the Trigger Manager via fast serial link (FSL). The FPTT board is a generic doublewide daughter board (DWDB). The FPTT has two Xilinx 600 FPGA chips in the U3 and U5 positions. The algorithms are implemented on the U3 chip alone.

Description of the algorithm

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		0	0	0	CR	FX	0	E	W	N	S	0	0	0	0	L1CIT/PS		DATA TYPE			L1/L2		
F2	0	0	0	HP	0	0	0	0	USH1		UMIP1		VSH1		VMIP1		USH0		UMIP0		VSH0		VMIP0		0	0	0	0
F3	0	0	0	HP	0	0	0	0	USH3		UMIP3		VSH3		VMIP3		USH2		UMIP2		VSH2		VMIP2		0	0	0	0
F4	0	0	0	HP	0	0	0	0	USH5		UMIP5		VSH5		VMIP5		USH4		UMIP4		VSH4		VMIP4		0	0	0	0
F5	0	0	0	HP	0	0	0	0	USH7		UMIP7		VSH7		VMIP7		USH6		UMIP6		VSH6		VMIP6		0	0	0	0
F6/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

Table 1 Protocol for LVDS transmissions between the FPSS and FPTT.

Each FPSS module sends four two-bit numbers from each of eight input links (sectors). This requires 4 frames as shown in Table 1. The four numbers characterizing each sector are *vMp, vSh, uMp, uSh*, where *vMp* is the number of v-oriented clusters with an associated *Mip* layer cluster, and *uSh* is u-oriented cluster with **no** *Mip* layer cluster, etc. The numbers have the following meaning: 00 – zero clusters, 01 – one cluster, 10 – two or more clusters, and 11 – error condition.
The first operation is to combine clusters in the *u* and *v* layers into an estimate of the number of objects. This is done in two ways to establish restrictive *(u* "and*"* *v*) and loose (*u* "or" *v*) definitions. The truth table for combining *u* with *v* is shown in Table 2.

U	00	00	00	01	01	01	10	10	10
V	00	01	10	00	01	10	00	01	10
UorV	00	01	10	01	01	10	10	10	10
UanV	00	00	00	00	01	01	00	01	10

Table 2 shows the truth table for object creation. UorV is the loose combination while UanV is more restrictive.

After the orientations are combined, each of the 32 sectors is characterized by four two bit multiplicities (*Mpn ,Shn*), where n=0-7. The next stage adds the numbers from four sectors to produce 2-bit inclusive quadrant sums, where a quadrant is ¼ of a side (North or South), and N=01 means 1 or more, and N=2 means 2 or more. The quadrant sums allow for 64 possible combinations: Side (2), Quadrant (4), *Mp/Sh* (2), *u* "and/or"*v* (2), Multiplicity (2). Any combination can be turned–on; however, the L1 trigger manager can accept at most 32 terms.

Sh U or V						Sh U an V					
	Mult=1			Mult=2			Mult=1			Mult=2	
Term	Side	Quad	Term	Side	Quad	Term	Side	Quad	Term	Side	Quad
32	N	0	40	N	0	48	N	0	56	N	0
33	N	1	41	N	1	49	N	1	57	N	1
34	N	2	42	N	2	50	N	2	58	N	2
35	N	3	43	N	3	51	N	3	59	N	3
36	S	0	44	S	0	52	S	0	60	S	0
37	S	1	45	S	1	53	S	1	61	S	1
38	S	2	46	S	2	54	S	2	62	S	2
39	S	3	47	S	3	55	S	3	63	S	3
Mp U or V						Mp U an V					
	Mult=1			Mult=2			Mult=1			Mult=2	
Term	Side	Quad	Term	Side	Quad	Term	Side	Quad	Term	Side	Quad
64	N	0	72	N	0	80	N	0	88	N	0
65	N	1	73	N	1	81	N	1	89	N	1
66	N	2	74	N	2	82	N	2	90	N	2
67	N	3	75	N	3	83	N	3	91	N	3
68	S	0	76	S	0	84	S	0	92	S	0
69	S	1	77	S	1	85	S	1	93	S	1
70	S	2	78	S	2	86	S	2	94	S	2
71	S	3	79	S	3	87	S	3	95	S	3

Table 3. FPQ trigger terms 32-95 are characterized by: Sh/Mp - the type of object, U an/or V - the type of combination, Multiplicity, Side, and Quadrant.

Frame	Second Byte								First Byte							
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F3	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
F4	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
F5	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
F6	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
F7/TF	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

Table 4. Protocol for data transfers form the FPTT to the L1 trigger manager by fast serial link,

The binary terms are mapped to the output frames as shown in Table 4.

Firmware Implementation

Figure 2 shows the top-level design of the FPTT. It is nearly identical to the CTTT, so only the differences are described in detail. There are four functional blocks
The *link_receiver* synchronizes the four input links to the board clock (link2 clock). The *slow interface* block allows input and output of control and monitoring information. The *L3 block* concatenates the L2 records and sends G-link formatted blocks. The *core block* encapsulates the trigger term construction and transmission format. With the exception of the number of input links (four), the only difference between CTTT and FPTT is the formation of the trigger terms.
Inside the *core* block is the *FPTT_terms* block as shown in Fig. 3, where the four input links carry information from NE, NW, SE, and SW detector regions (0-3 respectively). The *decoder* module stores the 4 data frames in registers. Then the total number of clusters with and without *Mip* clusters in computed for each of the *eight* quadrants. The four numbers are then reduced to a two-bit word corresponding to 0, 1, and 2 or more clusters (00,01,10). These are passed to the *addTerms* module, which forms the quadrant sums. The term bits are determined by concurrent examination of the quadrant sums.

L3 Output

Table 5 shows the format of the L3 transmission and Table 6 shows the data frame content. Each 28-bit LVDS frame requires two 16 bit G-link frames for transmission. Level 3 header frame six contains status information about the event.

bits(3 : 0) – event errors for links(3,2,1,0)
bits(14:0)='0'
bits(15) – OR of all error bits

Frame	CAV	DAV	FF	ED	Control Bits				Second Byte								First Byte							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
…	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
HF1	1	0	1	1	0	1	0	1	HEADER LENGTH								#DWORS MSB				#LVDS IN-LINKS			
HF2	1	0	1	1	0	0	0	0	HDR FORMAT				OBJECT FORMAT				#DWORDS LSB							
HF3	1	0	1	1	0	0	0	0	CROSSING NUMBER								L3 DATA TYPE							
HF4	1	0	1	1	0	0	0	0	TURN NUMBER															
HF5	1	0	1	1	0	0	0	0	FIRMWARE MINOR VERSION								FIRMWARE MAJOR VERSION							
HF6	1	0	1	1	0	0	0	0	L3 STATUS BITS															
DATA	1	0	1	1	0	0	0	0	DATA															
	1	0	1	1	0	0	0	0	DATA															
…	1	0	1	1	0	0	0	0	……															
	1	0	1	1	0	0	0	0	……															
TF1	1	0	1	1	0	0	0	0	L3 DATA TYPE								CROSSING NUMBER							
TF2	1	0	1	1	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP
PAD	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
…	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 5. Protocol for G-link L3 transfers from FPTT to crate 0x13.

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		0	E/W	N/S	#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	RA PSC FPS								PSC WIDTH			U/V	TS FPS				MIP	MIP BIT PATTERN						
…	0	0	0	HP	…….																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

Table 6. Protocol for L2 transfers between FPSS and FPTT.

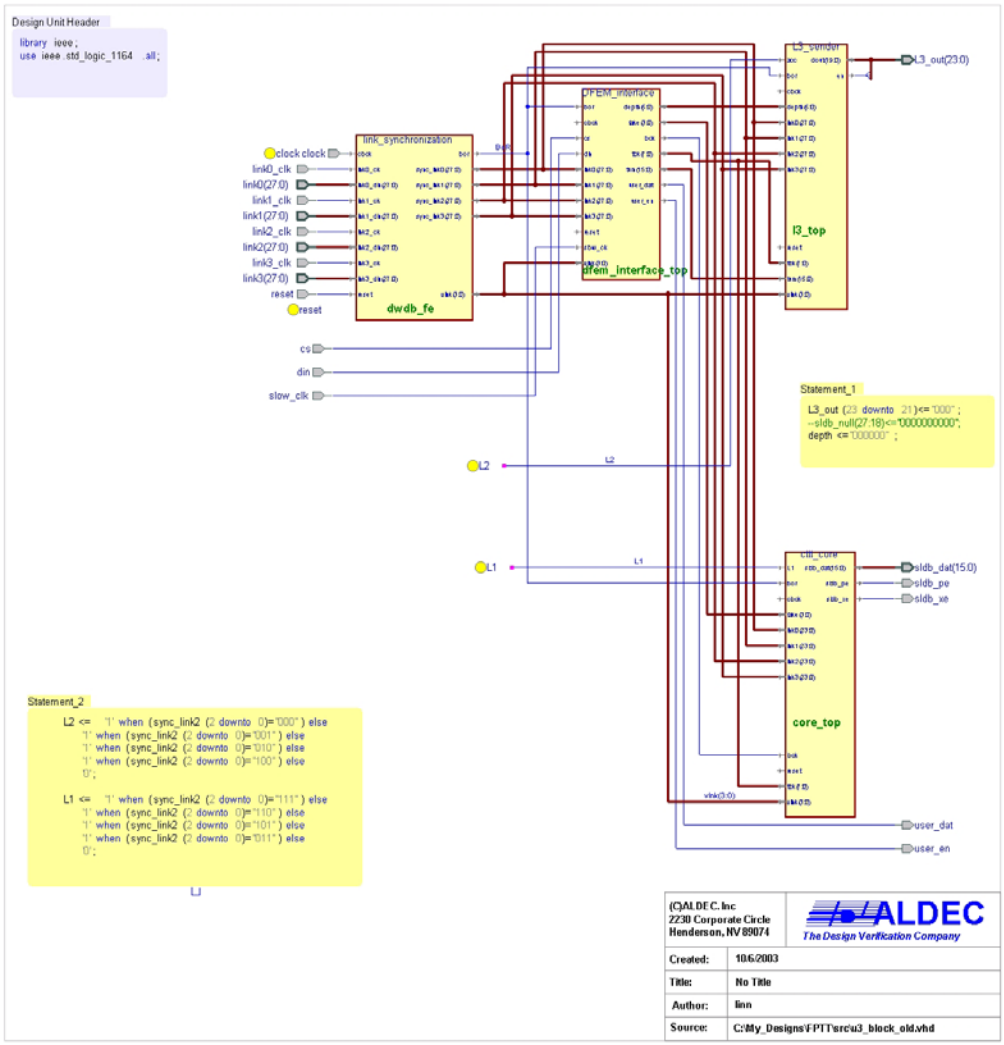

Figure 2 Top-level design of the U3 chip on the FPTT board.

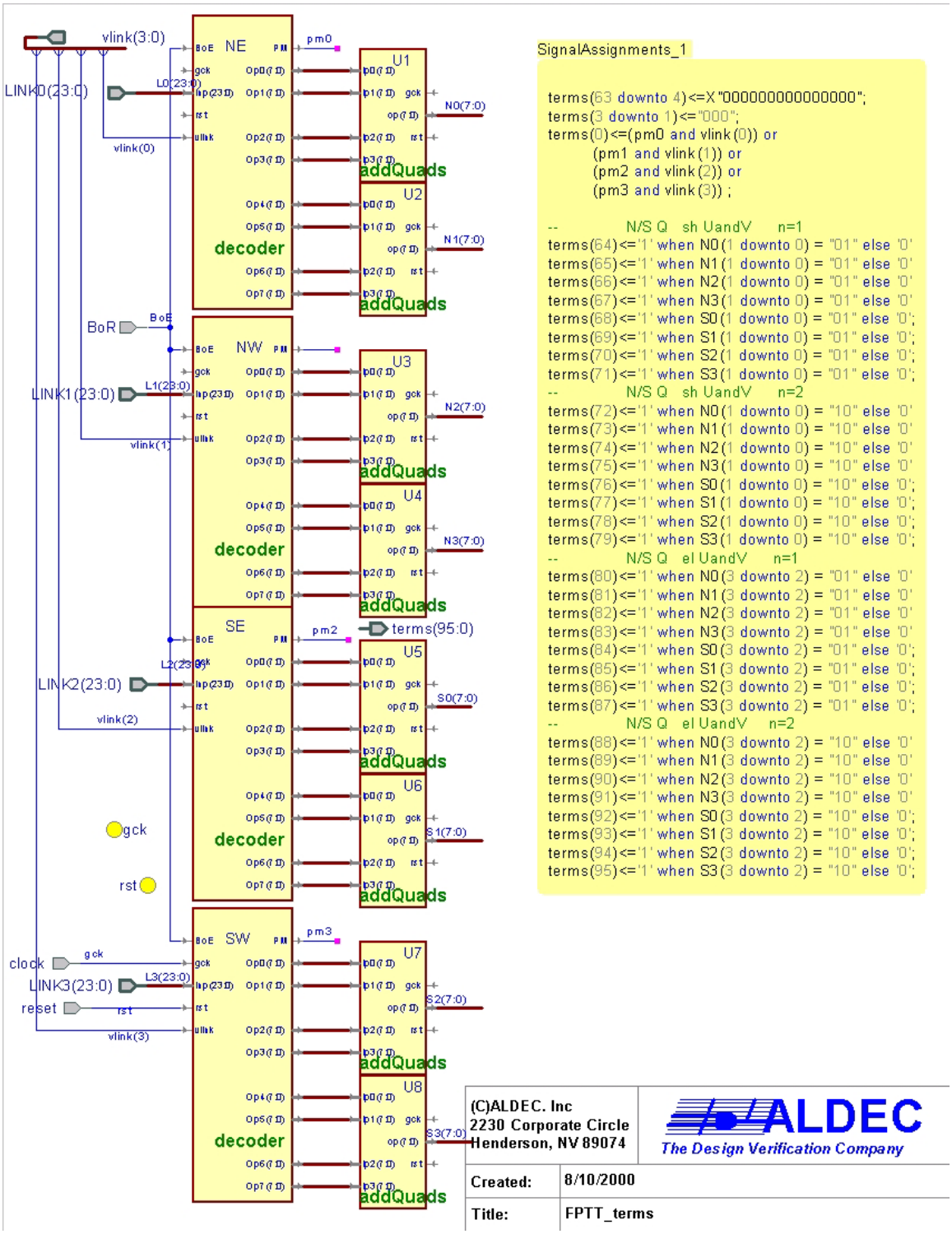

Figure 3 – the FPS_terms block diagram.

Slow Monitoring

page1 = 0x00
page2 = fake_register
page3 = depth_register
page4 = not supported
page5 = 0xAA
page6 = constant 0x55
page7 = not supported
page8 = missing link history
page9 = 0x0
page10 = sync history
page11= 0x0
page12 = parity history
page13 = 0x0
page14 = pattern history
page15 = 0x0 "00000000"